In the claims:

Following is a complete set of claims as amended with this Response.

1. (Original) A method comprising:

obtaining a processor tick counter value from a first processing engine;

comparing the obtained processor tick counter value to a processor tick counter value from a second processing engine; and

determining a timing offset for synchronizing the first processing engine and the second processing engine using the comparison.

2. (Original) The method of Claim 1, wherein obtaining a processor tick counter value comprises sending a request message from the second processing engine to the first processing engine, and receiving a reply from the first processing engine at the second processing engine.

3. (Original) The method of Claim 2, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the request message is sent.

4. (Currently Amended) The method of Claim 2, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the reply is received.

5. (Original) The method of Claim 2 further comprising repeating sending a request message, recording the time, receiving a reply, recording the time and determining a timing offset until the determined timing offsets are within a predetermined variability range.

6. (Original) The method of Claim 1 further comprising applying a time stamp to a message sent from the second processor, the time stamp being determined by applying the determined timing offset.

7. (Original) The method of Claim 1 further comprising receiving an instruction having an execution time and interpreting the execution time by applying the determined timing offset.

8. (Original) The method of Claim 1, further comprising:

obtaining a processor frequency from the first processing engine;

obtaining a processor frequency from the second processing engine; and

correcting the timing offset for any difference between the first processing engine frequency and the second processing engine frequency.

9. (Original) A machine-readable medium having stored thereon data representing sequences of instructions which, when executed by a machine, cause the machine to perform operations comprising:

obtaining a processor tick counter value from a first processing engine;

comparing the obtained processor tick counter value to a processor tick counter value from a second processing engine; and

determining a timing offset for synchronizing the first processing engine and the second processing engine using the comparison.

10. (Currently Amended) The machine-readable medium of Claim 9, wherein the instructions for obtaining a processor tick counter value comprise further instructions which, when executed by the machine, cause the machine to perform further operations comprising sending a request message from the second processing engine to the first processing engine, and receiving a reply from the first processing engine at the second processing engine.

11. (Currently Amended) The machine-readable medium of Claim 10, further comprising instructions which, when executed by the machine, cause the machine to perform further operations comprising determining the processor tick counter value at the second processing engine by recording the time at which the request message is sent.

12. (Currently Amended) The machine-readable medium of Claim 10, further comprising instructions which, when executed by the machine, cause the machine to perform further operations comprising determining the processor tick counter value at the second processing engine by recording the time at which the reply is received.

13. (Currently Amended) The machine-readable medium of Claim 9, further comprising instructions which, when executed by the machine, cause the machine to perform further operations comprising:

obtaining a processor frequency from the first processing engine;

obtaining a processor frequency from the second processing engine; and

correcting the timing offset for any difference between the first processing engine frequency and the second processing engine frequency.

14. (Original) A synchronized computing network comprising:

a first processing engine having a processor tick counter;

a second processing engine having a processor tick counter;

a communications link to send a value from the processor tick counter of the first processing engine to the second processing engine at one time; and

a processor of the second processing engine to compare the processor tick counter value from the first processing engine to a processor tick counter value from the second processing engine and determine a timing offset for synchronizing the first processing engine and the second processing engine using the comparison.

15. (Currently Amended) The synchronized computing network of Claim 14, wherein the first processor sends the processor tick counter value as a reply to a request message from the second processing engine.

16. (Currently Amended) The synchronized computing network of Claim 15, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the request message is sent.

17. (Currently Amended) The synchronized computing network of Claim 15, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the reply is received.

18. (Currently Amended) The synchronized computing network of Claim 14, wherein the first processing engine and the second processing engine run at different frequencies and wherein the processor corrects the timing offset for the difference between the first processing engine frequency and the second processing engine frequency.

19. (Currently Amended) The synchronized computing network of Claim 14, wherein the processor of the second processing engine applies a time stamp to a message sent from the second processing engine, the time stamp being determined by applying the determined timing offset.

20. (Currently Amended) The synchronized computing network of Claim 14, wherein the processor of the second processing engine executes an instruction at a time based on the determined timing offset.